FAMU-FSU College of Engineering

Department of Electrical and Computer Engineering

Final Fall Report

Team E#7

SAR Imager

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Date:

December 1, 2015

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Abstract

The Synthetic Aperture Radar (SAR) Imager senior design project, generously sponsored by Northrop Grumman, began in fall 2014 and seeks to develop a proof of concept prototype of a radar-based metal detection system for use in the security and military industries. This report outlines the fall 2015 team's evaluation of the current product, assesses major design challenges, proposes plans and rationale for redesign, and presents a strategy for completion.

1 Introduction

In partnership with the FAMU/FSU College of Engineering and Northrop Grumman, the objective of the Synthetic Aperture Radar (SAR) Imager Project is to develop a low-cost weapon detection system that provides suitable imagery resolution for physical security and military force protection applications.

Current detection technologies commonly employed in the security industry such as metal detectors, Advanced Imaging Technology (AIT) scanners, and x-ray scanners can be expensive, obtrusive, and require the subject to be inside the apparatus. An imager based on SAR technology, composed primarily of commercial-off-the-shelf (COTS) components, can be implemented at a lower cost than many industry-standard scanners; it may be placed behind a barrier, out of view from subjects; and most importantly, it can identify concealed metal objects from a distance.

In environments with multi-layered physical security protocols, the SAR imager's superior range can alert security professionals to potential threats before they reach an access control point, or before they progress further into a secure area, depending in which security layer the SAR is deployed. Some environments may be vulnerable to physical attack, but conventional AIT body scanners are too obtrusive or inefficient. An amusement park, for instance, might have high-level security needs, but their customers would not tolerate stepping into a full-body scanner.

Furthermore, random screening protocols have been widely criticized for being culturally or racially biased in practice. With SAR capability, guests can be discreetly imaged while queuing, and persons of interest can be identified for additional screening based on the presence of metal signatures rather than the caprice of a human screener.

2 Project Definition

2.1 Background

The 2014 FAMU/FSU College of Engineering & Northrop Grumman Synthetic Aperture Radar (SAR) Imager Project team laid the foundation for a successful radar imaging system. The 2015 team has inherited a wealth of technical documentation, including signal processing calculations; a fully-prototyped electrical system with all major components laid out for testing; and a functional, albeit simple, antenna structure. In 2014, the SAR team successfully transmitted and received a 20 ns wide RF pulsed signal at 10 GHz. Key capabilities not fully implemented in the 2014 design provide the starting point from which the 2015 project will build.

The Voltage-Controlled Oscillator (VCO) is not currently generating sufficient frequency to meet the passband frequency of the bandpass filter (4.631 GHz of 4.875 GHz required before multiplication). This is why the 2014 demonstration had to be done using an external signal source. The prototype must be able to generate its own signal, within calculated parameters.

The Field-Programmable Gate Array (FPGA) must provide precise, high-fidelity pulses to drive the switch that toggles between transmit and receive mode, and the switches that control which antennas are transmitting and receiving. The 2014 design partially demonstrated this capability by manually switching the FPGA using on-board slider switches, but a functional prototype must switch in real-time.

While the mathematical basis for signal processing functions has been set out, implementing these functions in software is quite another task. The SAR must be able to resolve the reflected signals into useful data. After this problem is solved, that data must be parsed to illuminate the pixels of a VGA display, another challenging programming problem.

Finally, the existing antenna structure needs to be redesigned with emphasis on weight-reduction, mobility, precision and repeatability of alignment, rigidity, and practicality.

The SAR imager design uses the reflection of radio frequency (RF) waves to create an image. Much in the way a bat sends pulses of sound and listens to the reflected echoes to determine the

distance of objects, the SAR emits pulses of RF, and “listens” for amplitude changes and phase shifts in the reflected signals to determine the distance and composition of objects.

Typical SAR systems are airborne, using the aircraft’s movement to synthesize a much larger antenna. The FAMU/FSU and Northrop Grumman Stationary SAR Imager uses an array of small antennas to synthesize a large virtual antenna with no moving parts. This proof of concept prototype will cast a 40 square inch imaging scene at a range of 20 feet.

2.2 Objectives and goals

The system-level objectives for Semester I are focused on assessing the Generation 1 product, developing design improvements that will add value and functionality to the product, and developing clear, achievable strategies for fabrication and implementation in Semester II.

Verifying the current electrical system is the first, essential step to setting the foundation for future improvements and redesign. To that end, the team will perform an exhaustive battery of tests to isolate faulty components and identify potential areas of improvement or redesign. The first battery of tests is described in test plans seen in Appendix A (A3 – A4). Tests will be carried out according to a test plan standard operating procedure which is a hybrid of IEEE 829 Standard for Test Documentation and Northrop Grumman testing procedures. Given the uncertain nature of testing, estimates for what tests will be completed by the end of Semester 1 are probably optimistic, but the ideal goal is to test output through the transmit signal path without FPGA timing, and to troubleshoot the currently malfunctioning VCO.

A considerable amount of FPGA code needs to be written and debugged in order to achieve independent functionality. The software development strategy revolves around progressing from the system level, down to the code. Sub-module diagrams and pseudocode will be completed by the end of Semester I so that team members can work on their coding assignments over the break. The mechanical redesign is being led by ME Team 18, in close collaboration with ECE Team 7. Designs will be finalized and materials ordered by the close of Semester I in accordance with ME Team 18’s deadlines.

3 Design and Analysis

3.1 Functional Analysis

The team will deliver a functional SAR imaging prototype that fulfills the requirement specifications as well as all appropriate supporting documentation including a user manual with troubleshooting flowchart(s) and component specifications.

3.2 Design Concepts

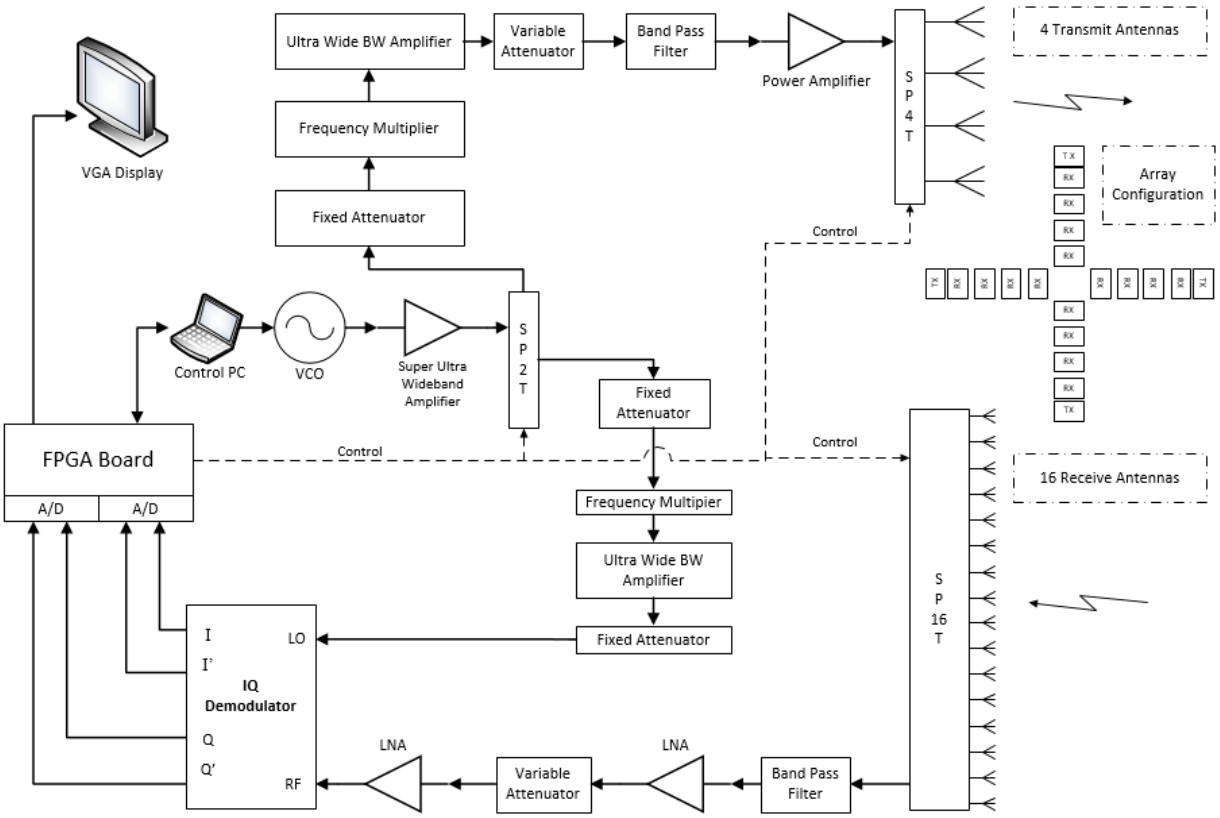

Figure 1 – System level block diagram

3.2.1 Signal Processing and Image Formation

In Synthetic Aperture Radar Imaging, Signal Processing is the key to actually decomposing the signal of the electromagnetic pulse and then finally forming the scene being captured into an image. The first major key technical question that must be asked is why the team actually needs to implement the Fourier transform? The Fourier transform is one of the key techniques that is used

in almost all signal processing. The Transform will be able to take the signal, pick up different energies and distances once put through the transform, then using this data, be able to form a certain scattering of these energies and give all of the necessary information to generate the image that was captured at the scene. Specifically, the transform is used to decompose the signal into different sine and cosine waves. These then are read as in-phase (I) and quadrature (Q) values, which will be compared to basic functions, or I and Q values from the original transmitted signal.

Now one important note to make is that the Fourier Transform is most often used to transform signals that were once in the time domain into signals in the frequency domain, which allows for much simpler manipulation and analysis of the signal. This will be a discrete Fourier Transform, with the I and Q values being taken from the basis functions and the received signal. a key goal of the project is to then implement the Fourier Transform on the FPGA. In particular, the Discrete Fourier Transform for this system will just be separate complex multiplications of the in phase, or "real", components of the received signal after being passed through the demodulator on the receive chain and the real part of the transmitted signal, then another set of complex multiplications for the quadrature, or complex, parts of the received signal and the transmitted signal. These sets of complex multiplications will be done for all 16 phase centers, or the 16 different signals that are received that correlate to the 16 different transmit-receive pairs of the system, which then describe the different areas of the scene being targeted. The reason this complex multiplication is being done is to solve the problem of how to detect different energy levels of a scene in order to detect and image the metal that is being targeted. The 16 different phase centers are representative of the 16 separate transmit-receive pairs of the radar system and the areas of the scene that these phase centers are correlating to. The phase centers are represented as functions in the form of:

$$f(\theta_i) = dsin(\theta_i) \quad (1)$$

In this function, the value θ_i is the phase angle of any of the 16 phase centers, where i describes the number of the phase center. The value of d describes the distance of the current phase center from the center phase center. These 16 different functions are the 16 reflected signals off of the target that are being received which will be decomposed into their respective in phase and quadrature components. After combining the resulting in phase and quadrature components of the 16 different phase centers, as a result of performing the complex multiplication, then

converting that amplitude to the Decibel (dB) Scale, an energy scatter plot can be made to see the different energy levels of the targeted scene. A sample plot can be seen below:

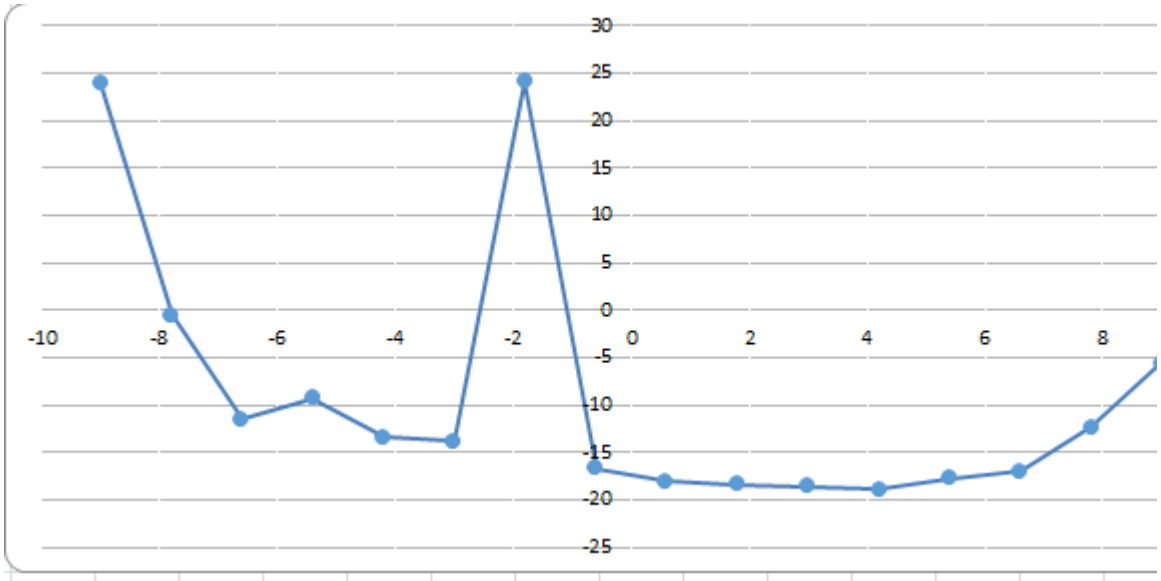

Figure 2- Amplitude of Energy vs Phase Center

Whenever there is a peak in the energy relative to the rest of the phase centers, as can be seen at phase center #7, then some metal is being targeted at the location of the scene. On the topic of degrading lobes, the peak shown at phase center #1 is actually a result of what is called ghosting. When a phase center is positioned at more extreme angles away from the scene being targeted, the reflection of the received signal can actually create a "ghosted" image, or a spike in the amplitude of the energy at that phase center, when in fact, this energy level does not actually exist. When the phase angle is considerably extreme compared to the rest of the phase centers, reflections of the signal at other phase centers can accidentally appear due to the existence of side lobes outside of the main antenna radiation pattern. Because the phase centers on the outside of the energy scatter sit on the edges of the main lobe of antenna radiation, ghosted images from the side lobes can appear. During the image processing of the system, one solution that can be designed is simply coding a case that checks if some energy peak is being observed at an extreme phase center when the actual energy peak is at a non-extreme phase angle, and if this is the case, then the code can tell the display not to show the ghosted image at the extreme phase centers. An example of an antenna radiation pattern in Cartesian form showing the main and side lobes can be seen below:

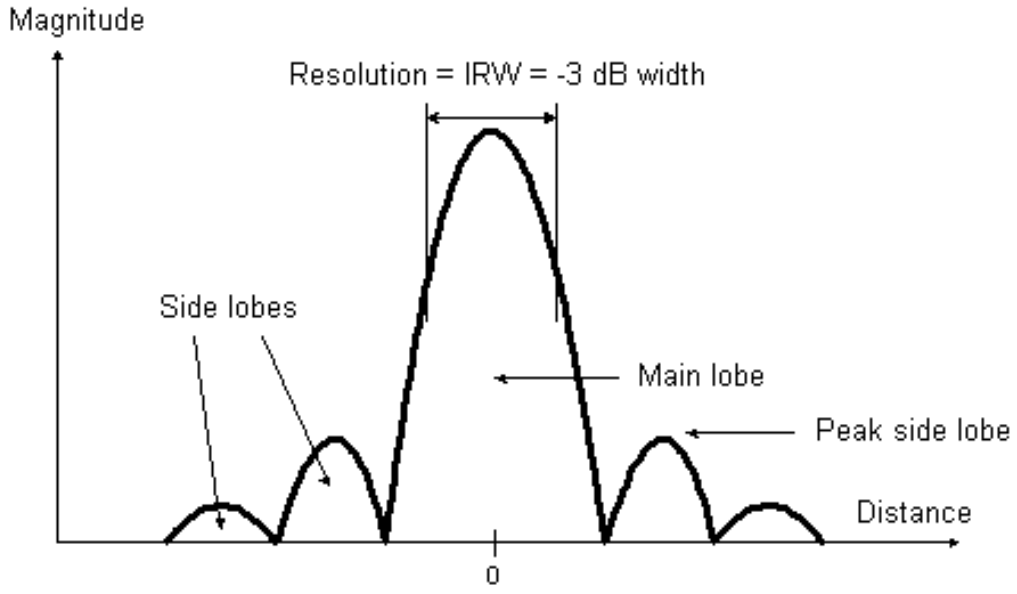

Figure 3 - Degrading lobes

From the phase center relative amplitude values, the image processing can then be implemented using VHDL, which will be described about in more detail later on in the Software Development section. The display screen will then display 16 different segmented out sections of the screen that will then light up, or "turn on", to indicate which of the 16 different phase centers has an energy peak. This allows the system to visually indicate at which phase center some metal is being detected. Because the energy scatter plot cannot be formally produced using the FPGA board, and the budget constrains the resolution that is possible with the imaging, the 16 segments of the VGA display screen was the team's design solution to the image processing.

Now the biggest question is how the complex multiplication will actually be calculated on the FPGA board. There were two solutions to this problem. The first was being to purchase a Fast Fourier transform (FFT) module that is compatible with the FPGA board that can perform many different complex multiplications in a fairly short amount of processing time. The other option was to independently develop or research an algorithm that can be implemented using VHDL code and perform the complex multiplication using the FPGA's native computation processing. The downside to the second option is that it would take much more time to develop an algorithm and implement it on VHDL than it would be to order the separate module and spare a lot of VHDL coding. Using code on the FPGA board that was developed from an algorithm will also take more

processing time to do all of the calculations than the time it would take the FFT module to do all of the signal processing calculations. However, the decision to go with the second option of developing and implementing an algorithm to do the complex multiplication was chosen because the FFT module would cost roughly $2000 dollars, while developing an algorithm would be free. Staying under budget and presenting a cheaper option is a much larger priority for the team and the sponsor than to achieve quick signal processing times at this stage in development. This also provides a more valuable educational experience in engineering algorithms that can be used for signal processing than letting a module do all of the hard work, leading to more intimacy with the project as a whole. An algorithm was actually found in Dr. Uwe Meyer-Basae's book "Digital Signal Processing with FPGAs" and has been decided that it can be implemented in VHDL. This algorithm is shown as follows:

$$s[1]=a-b; \quad s[2]=c-d; \quad s[3]=c+d;$$
$$m[1]=s[1]d; \quad m[2]=s[2]a; \quad m[3]=s[3]b;$$
$$s[4]=m[1]+m[2]; \quad s[5]=m[1]+m[3];$$
$$(a+jb)(c+jd) = s[4]+js[5];$$

Figure 4 – Complex multiplication algorithm

This algorithm actually makes it possible for an FPGA to perform a complex multiplication of two complex signals, in the case of this project's signal processing, the received signal of a phase center, which is represented by (a+jb), where a is in phase part and b is the quadrature component, and the original transmitted signal of a single phase center which is represented by (c+jd), where c and d are the in phase and quadrature components, respectively. The result of the complex multiplication of the two complex functions is represented here by s[4]+js[5], where s[4] and s[5] are, respectively, the in phase and the quadrature components. In order to get to this point, s[4] is the sum of (ad-bd) + (ca-da), and s[5] is the sum of (ad-bd) + (cb +db). This is done to represent both the real and complex components of the final signal, because the FPGA board cannot handle complex multiplication without mathematical manipulation, which this algorithm actually does. Moving forward, this must be implemented using VHDL for all 16 phase centers, which is estimated to be done very early during the Spring 2016 Semester, or even during Winter Break.

One important design factor that should be noted is that the values for c and d, or the in phase and quadrature components of the basis functions (transmitted signal), will be stored as constants in memory on the FPGA board. This can be done because these basis functions will never change, as the system will also transmit the same signal. The a and b values, or in phase and quadrature components of the received signal after demodulation, will not be stored in memory because these values will change depending on the signal being reflected back. To briefly touch on the topic of cluttering, or reflected signals that are bouncing off of external sources that are not the target, such as walls behind the targeted scene or even the floor. The plan to reduce this would be to surround the 20 foot distance where the metal is being targeted with RF absorbing material to mitigate the amount of multipath interference that is a result of signals reflecting off of other objects not in the scene.

3.2.2 Noise Considerations

The noise will also have to be taken into consideration when designing and analyzing the system used. This is important because noise can create uncertainty in signals, making analysis of these signals much more difficult, and in times where the noise is very high, almost impossible. The Signal to Noise Ratio (SNR) is given by the equation:

$$SNR_{dB} = \frac{Signal\ Power_{dB}}{Noise\ Power_{dB}} \quad (2)$$

Essentially, the higher the SNR, the better the signal will be when compared to the noise that also is received. As of right now, the SNR of the entire system after budget analysis performed by previous team is about 55 dB. Moving forward, the team will improve upon or at least maintain the current ratio by keeping the components on the receive chain as close to the antennas as possible. One way that the incoming noise is being reduced is by sending the signal through a band-pass filter at the very beginning of the receive chain. Typically, the filtering process happens before the amplification of the signal, which is used to more easily process a signal. In the imager that is being used by this particular team, the amplifier on the receive chain after the band pass filter that is being used is a low noise amplifier (LNA) which will amplify the received signal while adding a small amount of noise to the system. The LNA is necessary for

the design of the system because it will amplify the received signal to a higher power amplitude. Without this amplification, the In Phase and Quadrature Demodulator, as seen on the bottom portion of figure-1, the block diagram, cannot operate due to technical specifications given by the manufacturer. Without the signal going through demodulation, signal processing will be impossible and no image can be formed. The extra amount of noise added to the system from this one amplifier is not nearly as important as being able to perform the signal processing, so some concessions had to be made.

The issue of noise has already come up in the engineering decision process between the electrical engineering led team and the mechanical engineering led team. The Mechanical Engineering Team actually proposed moving the component box from the frame's cross section, down to the base of the frame, in order to reduce the center of mass. The issue is that it would require the SubMiniature version A (SMA) connecting cables from the receive antennas to the 16 way solid state switch in the component box to increase by a length of roughly 3 feet for each of the 16 cables. This increase in path length allows for more noise interference through the cables; a potential problem for the signal analysis. The team must consider if it is actually worth moving forward with this option, if it actually impacts the RF receive chain too much. One way to combat this is place the filter and the Low Noise Amplifier much closer to the cross section and in its own small component box away from the main box. Noise from ohmic devices after the LNA are insignificant compared to the signal gain from the LNA.

However, another option is being explored with the mechanical engineering in charge of designing the new component box. The new design would just be to just have the component box positioned directly onto the back of the cross section on top of the back support legs, where the Bandpass Filter and the first Low Noise Amplifier on the receive path would be situated on the side of the box closest to the cross section in order to mitigate the path length between the antennas and the LNA. This option is most likely going to be taken because it will make the fabrication of the component box cheaper and easier to fabricate than to have two separate component boxes as would be necessary in the first option presented, while also not majorly affecting the SNR of the system as a whole. The calculations for noise power of the system can be seen in the following equation for the cascaded noise figure of a system:

$$F_N = F_1 + \frac{F_2 - 1}{G_1} + \cdots + \frac{F_N - 1}{G_1 \ldots G_{N-1}} \quad (3)$$

where FN is the noise figure for the overall system, F1 is the noise figure for the first component on the signal path and G1 is the gain of the first component on the signal path. Moving forward, RF Noise budgets will be produced for the entire system. Last year's team constructed their own, but upon review, it was found that this budget spreadsheet was incorrect for some of the noise gains due to calculation error. This is why one of the goals by early Spring Semester is to have the RF Noise budget spreadsheets to be completely reworked for the current electrical system. The radar equation will also be used to measure the received power, which is given by the equation:

$$P_r = \frac{P_t G_t A_r \sigma F^4}{(4\pi)^2 R_t^2 R_r^2} \quad (4)$$

Where P_r is the received power of the system, Pt is the power of the signal at the transmitting antennas, $G_t$is the gain of the transmit path, A_r is the surface area of the transmit antenna and the values of R_r are given by the distances that the signal travels on each path.

3.2.3 Software Development and Implementation Analysis

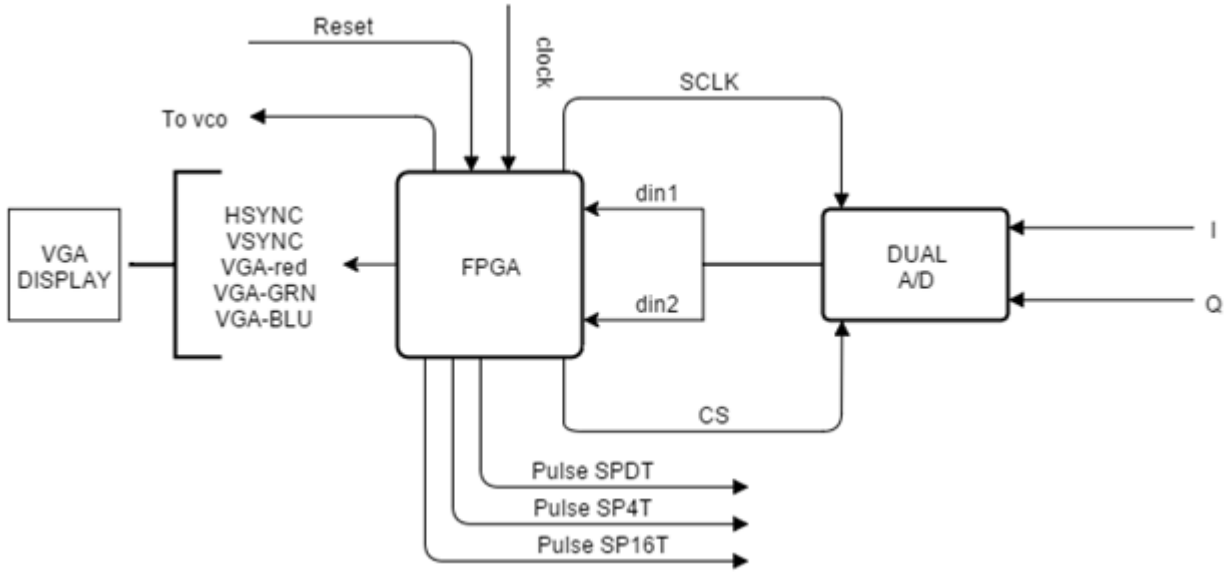

Figure 5 - Top-Level Design Diagram

The radar system will be using the NEXYS 3 Diligent board which uses the Xilinx Spartan 6 FPGA chip. The FPGA board is equipped with PMOD port, VGA port, and a USB port. The PMOD port will be used for the connection between the board and the ADC components –also

from Diligent manufacturer. The operation of the radar depends on the underlying software of the FPGA. The FPGA will be "talking" to different components of the radar system, such as the voltage controlled oscillator (VCO), the analog-to-digital converter (A/D), the switches, and the VGA output of the monitor. A complete top level-design is shown in figure-5. This diagram shows where the input/output of each module, and how each module interacts with the other.

Special attention is required in the development of the software. The team has divided the FPGA programing into four main modules:

1) Signal generation and radar system timing module
2) Analog to digital conversion module
3) Mathematical calculation module
4) VGA display Module.

3.2.4 Signal generation and system timing module

SAR radar is a synchronous system. Each component in a radar is required to be only active for a certain amount of time. This module is responsible of controlling the different switches on the antenna. The SAR radar will function under two modes. Transmitting mode refers to the period of time when a signal is sent from the antenna to the target. Receiving mode refers to the period of time when the signal is bounced back to the receiving antenna, this mode also includes the signal processing of the data from the receiving antennas. Changing between receiving mode and transmitting mode is crucial because delay in the switches will result into attenuation of the data collected. This module will need to successfully time the switching frequency between the transmit path and the receive path. This path is controlled by the SPDT switches. In addition, this module will also time the switching frequency of the SP4T and SP16T switches which controlled the data at the 4 transmitting antenna and the 16 receiving antenna respectively.

In order to solve the system timing issue faced by the 2014-2015 SAR team, this module will also include the clock signal for different modules such as the ADC module, and the VGA module. The thinking behind doing one module for all clock signals is that it is much easiest to adjust the timing by having one VHDL code dedicated specifically for that purpose.

To accomplish the timing of all the clock signal, the software will use the 100 MHz clock of the NEXYS 3 board. The clock will be sampled at every two rising edge in order to get the 50 MHz signal that will drive the Transmit-Receive switch. This 50 MHz pulse will have a 0.333 duty

cycle (i.e. the clock will be active for 20ns and off for 40ns). The reason behind selecting 20ns as the active time of the pulse is because it takes about 1ns per foot for the RF signal to travel in the medium. Since the target is positioned at 20 feet away of the antenna, 20ns is required for the pulse to reach the target. During the 40ns period, the radar system will be in receiving mode. 20 ns of the 40 ns is dedicated for the signal to travel back to the transmitter. And the other 20 ns will be used for signal processing and for components time delay that may occur. The 100 MHz clock of the NEXYS 3 board has a period of 10 ns. The clock edge can be monitored in order to switch components every 10 ns. Additional delay occur when the signal rise high and settle low. Therefore, the switching speed of the system is a combination of rising time, settling time, components delay, and external factors such as cable path interference.

Implementing the code for this module can be accomplished easily using the core generator of XILINX ISE Design Suite 14.4. This feature can be found under ToolsàCore generator. From there one can access the wizard user interface by doing the following click: FPGA Features and DESIGN→clocking→ Clocking Wizard 3.6. This feature simplifies the creation of HDL source code customized to the circuit clocking requirements.

The Nexys3 board has two types of connector: 68-pin VHDC connector for high-speed/parallel I/O and 8-pin Pmod connector for lower speed and lower pin-count I/O. The VHDC connectors include 40 data signals that can accommodate data rates of several hundred megahertz on every pin. The VHDC ports will be used for the switch signals – precisely, the Single Pole Double Throw toggle (SPDT) switches since that signal will have a frequency of 50MHz.

Figure-6 shows a possible timing diagram for the System timing module. The team will have to change delay time if the assumed time is not enough or if it is too much. This can be achieved only through testing. However, the task of changing the signal frequency and duty cycle is simple because all of the signal is only controlled by the timing module. Figure-7 is the predicted block diagram for this module.

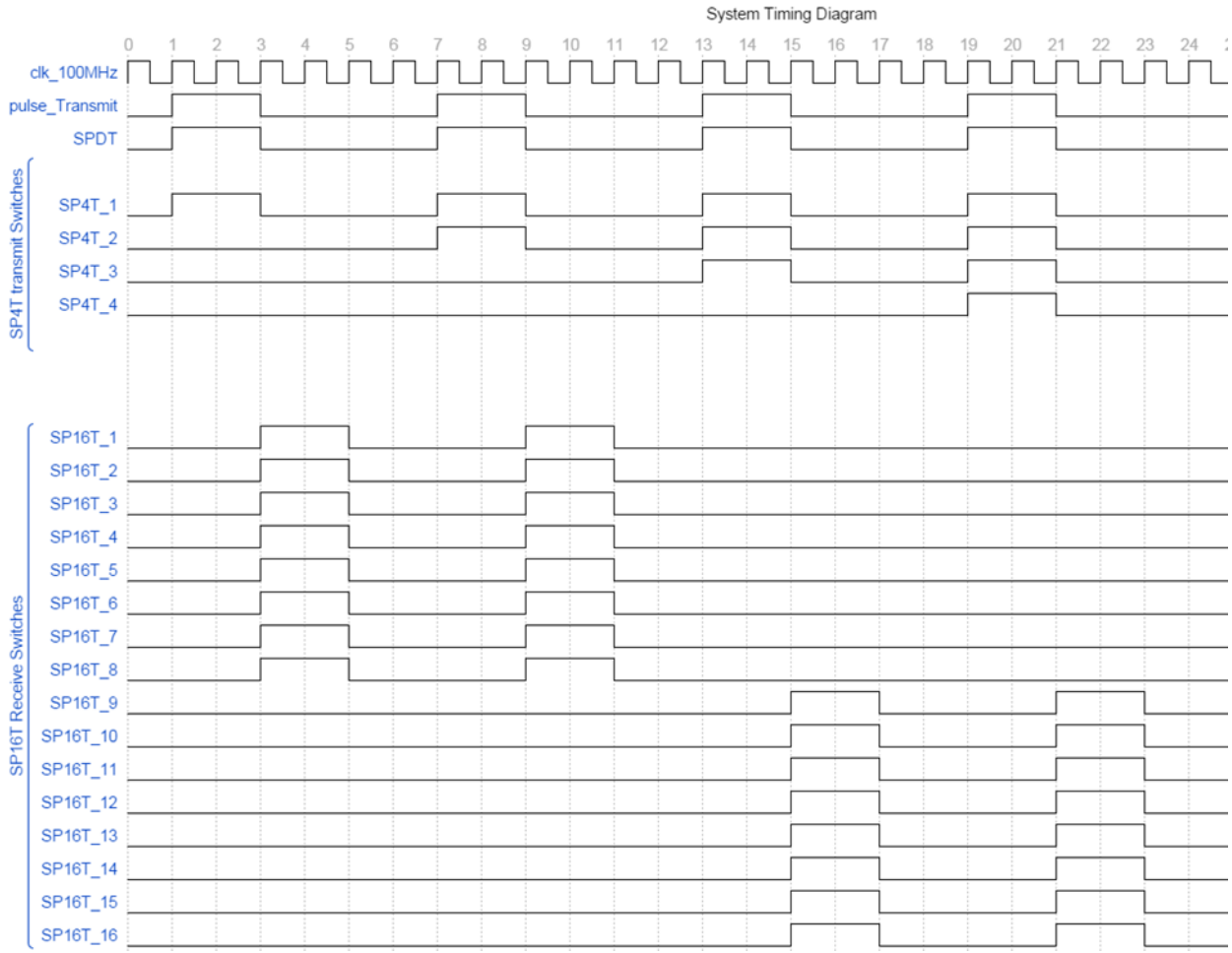

Figure 6 – System Timing Diagram

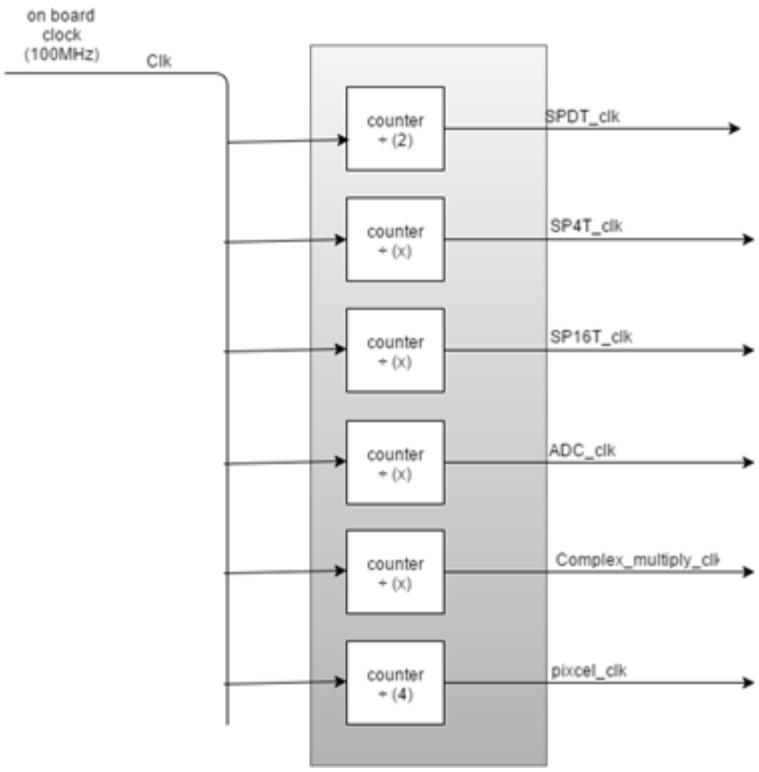

Figure 7 – Predicted Block Diagram System Timing Module

3.2.5 Analog to Digital Conversion Module

This module is required to change the analog signal coming from the In-phase and Quadrature-phase demodulator (IQ demodulator) into a 12-bit digital signal that will later be processed in the FPGA. The Pmod connectors, used for lower frequency signals, will be used for the A/D connector. A block diagram of this module looks as follow.

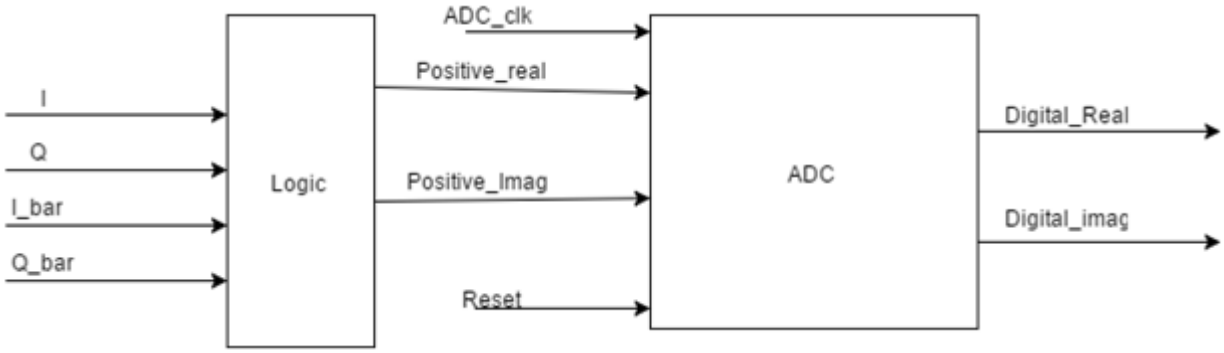

Figure 8- Predicted Block Diagram for ADC module

The PmodDA4 ADC device from diligent will be used to communicate with the NEXYS 3 board. This component is shown in figure-9. A logic circuit is required at the input side of the ADC module because the IQ demodulator output signal range from -8mV to +8mV. The PmodDA4 ADC device only accept voltage range from 0 to 3.3 Volt. The complex conjugate aspect of the I- I` and Q - Q` signals is utilized to design a circuit that will only take the in positive value. The logic for this block is as follows:

```
IF I=0 and I_bar≠0
        Then I = - I_bar
Else IF i_bar=0 and I≠0
        Then I_bar = - I
```
similar thinking is applied to Q and Qbar

Figure 9- A/D Convertor from Diligent

3.2.6 Mathematical Calculation Module

In terms of signal processing, there exist basis functions that need to be multiplied with the different I and Q values from the IQ demodulator. Those basis functions are pre-calculated. A complex multiplication is used to find the peak amplitude and phase information of the receiving signal. A need to store the base functions is obvious. Since VHDL is a hardware description language, creating variables to hold the basis information is difficult. A complete block diagram for this module is as follow.

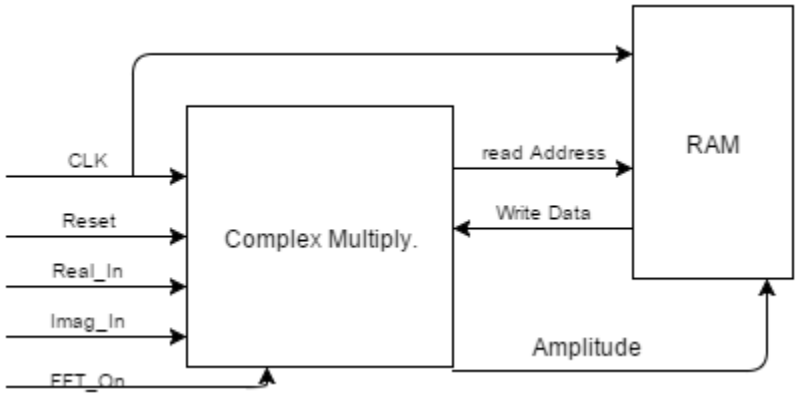

Figure 10 – Top-Level Function Diagram

The 16Mbyte Micron Cellular RAM will be used to store the base function. With this memory in place, calculation can be done easily using VHDL. The output of the module can then be used to calculate the amplitude and phase of the radar signal coming from the IQ channel. These values can then be stored in the RAM for later use by the VGA to output to a display. The 16Mbyte Micron Cellular RAM is complex. Detailed information about the signal flow is presented in the appendix A-6.

3.2.7 VGA Display Module

The VGA standards were originally developed by IBM and allow for a display resolution of 640x480 pixels. For any VGA application, two kinds of VGA interface signals needs to be displayed. The first one is the data signal which is composed of the red, green and blue signals.

The second is the control signal which is composed of the horizontal synchronization (HS) and vertical synchronization signals (VS).

For the imaging, we will divide the 640x480 pixels frame into 16 regions. Each region will have a color configuration based on the peak amplitude of the receive signal at each of the 16 receive antenna. The peak amplitude was calculated in the mathematical calculation module. In order to implement this code, the team will implement 2 submodules

1) The Timing Control Module.

The timing control module is a key part of the display controller. It will control the VS and HS signals. These signals determine what pixel region is being used.

2) VGA Display Controller Module.

This module will assign the RGB value for each region.

A complete block diagram for this module is as follows.

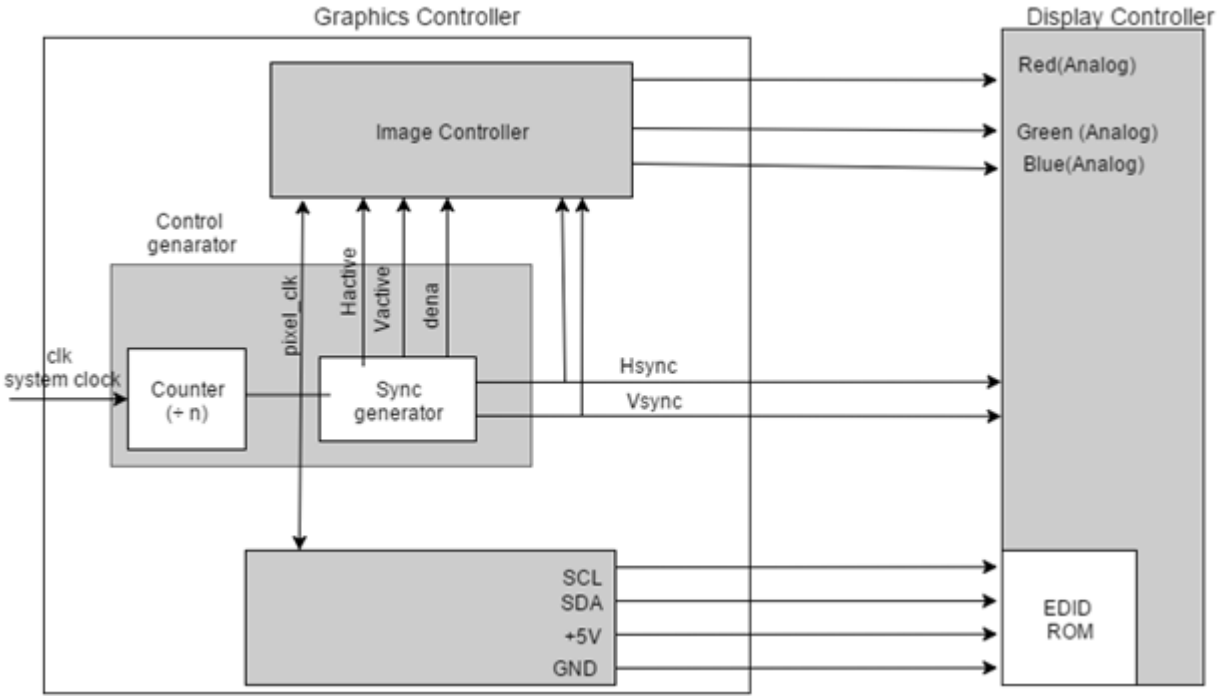

Figure 11 - Predicted Block Diagram for VGA Module

3.2.8 Structure

Figure-4 shows the prototype that the 2014 team produced. Currently, this structure is over 200 pounds with the component box attached. The structure's height is 60" and its width is 61". It

is made from ¼" steel, which is the main reason for the structure's excessive weight. The loose tolerances between the structural components and lack of adequate bracing causes wobbling when touched. This instability may compromise RF calibration.

For these reasons, the customer requires a complete structural redesign to optimize stability and reduce weight. A further point of interest would be to increase the mobility of the prototype. As one can see from the image, there are no options for relocating the structure aside from lifting it. This is especially cumbersome due to the structure's extensive weight.

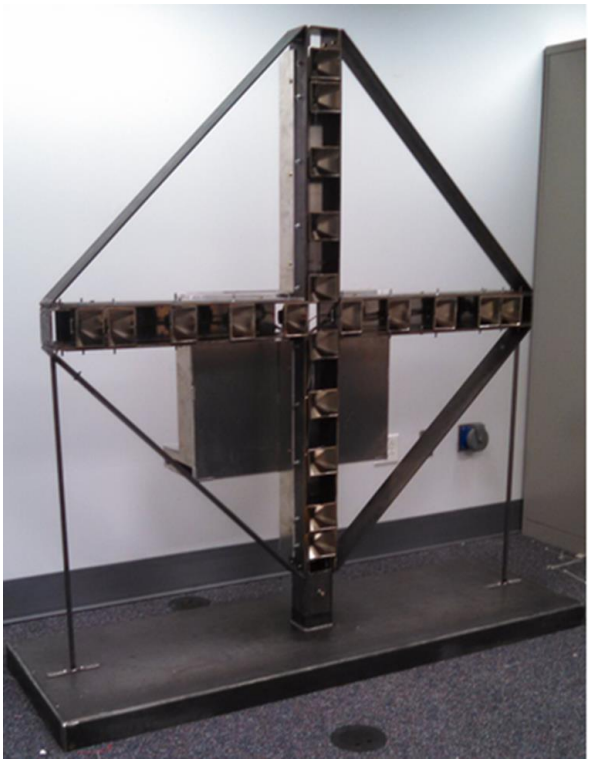

Figure 12 - Gen 1 structure

Gen 2.1 Structure

The Gen 2.1 structure will be made of 80-20 series 10 aluminum which is a commercial off the shelf product seen in figure 14. This extruded material weighs only 0.5lbs per foot allowing us to meet the 80 lb. weight limit. This material will also allow for limitless translational horn placement. Additionally, this material is modular, minimizing machining requirements while simplifying the assembly and installation process. Unfortunately this design will consist of many

1/8” fasteners. Which may shear due to the weight of the component box or the due to a large force. This design offers little protection to the wires or the wave guides. Finally it will not allow for finite translational adjustments for the horn holders.

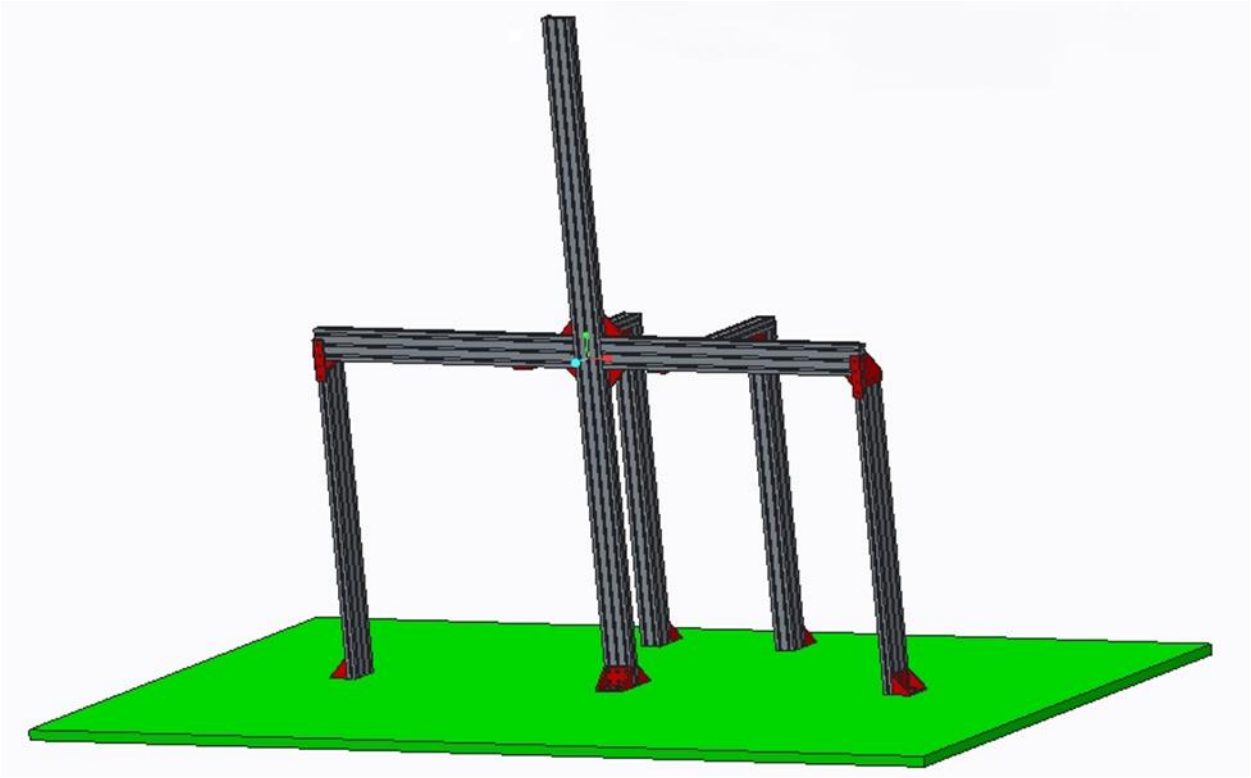

Figure 13 – Cad image of the new frame design

Figure 14 - Image of 80/20 series 10 cross section

Gen 2.2 Structure

After talking with our sponsor, it was determined that the ability to mount the radar into a wall would be an advantageous design concept. This solidified the decision to use the 80/20 series erector set because it is easy to disassemble down to the basic cross that can bolt into a wall. When the design for the horn holders was finalized it was apparent that the series 10 80/20 would not be sufficient for the cross section of the radar. Therefore the decision to move to series 1545 80/20 was made which can be seen below in figure 15. Which allows for easy horn installation, reducing the time needed to assemble the new system.

Figure 15 – Image of the cross section of 80/20 series 1545

Once it was confirmed that the new series of 80/20 would work, the decision to add castors to the structure were necessary to keep allow for easy transportation of the radar. Therefore additional reinforcement was required to keep the structure stable against torsional forces. This was done by adding additional support legs on the outside of each arm parallel to the ground, along with a box frame along the bottom that will allow for easy installation of the castors. This design change can be seen below in figure 16.

Figure 16 – Gen 2.2 Structure Design

Once the frame design was completed, all the horns were mounted to the new structure design to verify that everything would fit together correctly. The spacing between the horns was kept the same as the first generations, which is 3 inches between the send antennas and the first receive antennae, then 6 inches between each of the remaining receive antennas.

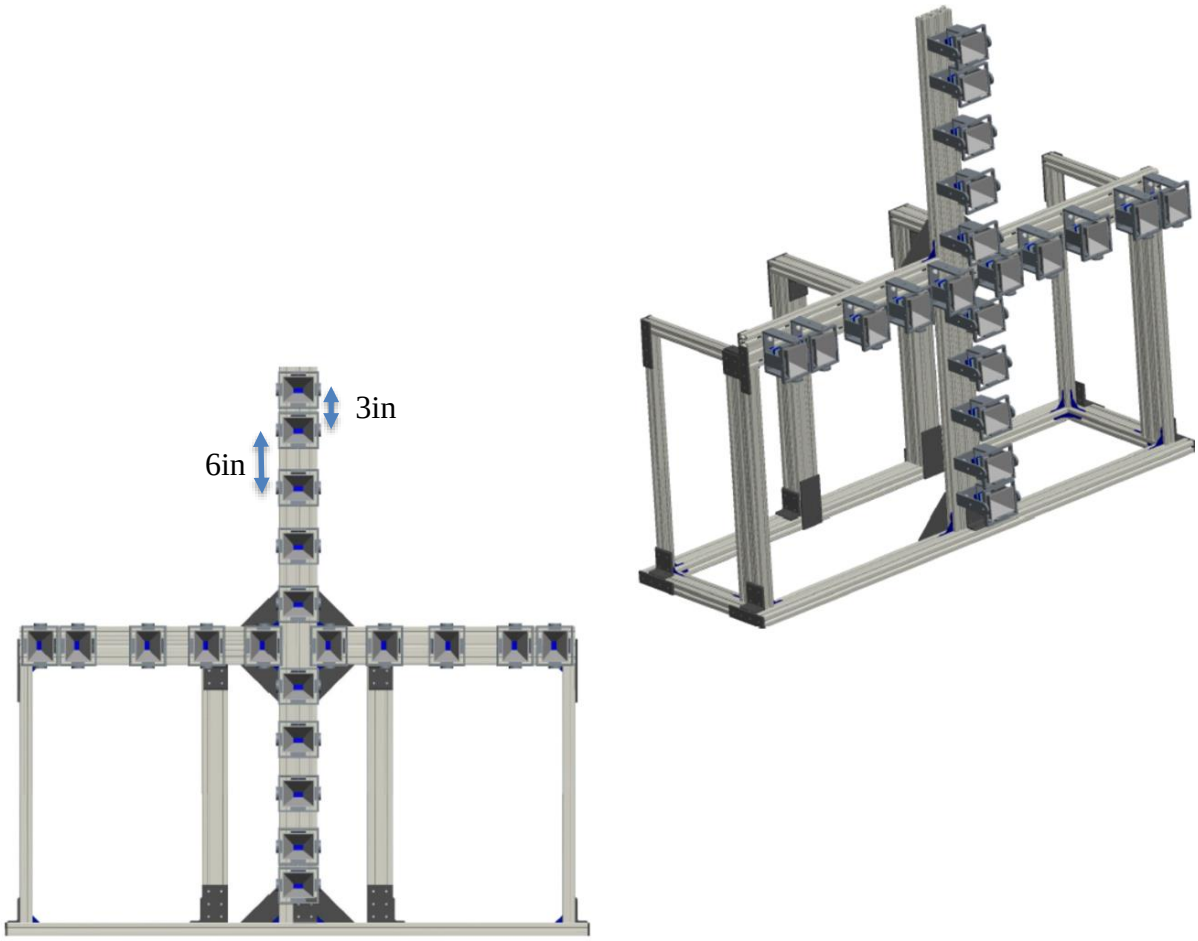

Figure 17 image of the completed assembly

3.2.9 Horn Holders

The horn holders act as the housing and the adjusting platform for the horns which emit and receive the radio frequency signal. It is imperative that this action functions properly and that the error in the accuracy should be minimized. The horn holders should allow the user to seamlessly calibrate the horns, secure their position when required, and be able to adjust them if needed. The horn holder design from the 2014 team is in need of a complete redesign. This design only allowed for one degree of freedom. Northrop Grumman has stated that the horn holders must possess two degrees of freedom (Azimuth and Elevation).

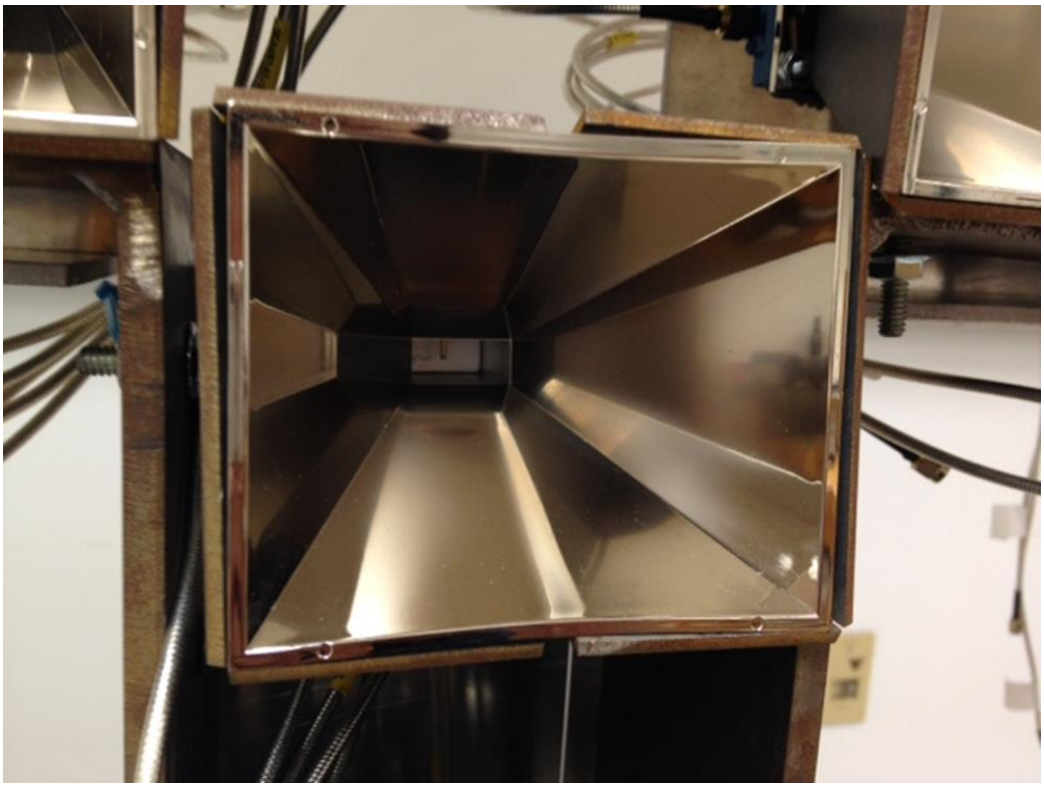

Figure 18 – Gen 1 horn holder, notice the deformation along the bottom of wave guide

Above in Figure-18 the current horn holder is displayed. This shows how the holder is a shell that is screwed into the antenna structure. The horn sits within the shell and is rigidly attached to structure once the shell is screwed in. The horns in the horizontal array can only have the azimuth angle adjusted whereas the horns in the vertical array can only have the elevation angle adjusted. This limitation in movement is due to shells fitting along the ¼" steel -frame.

Another point of concern lies within the actual adjustment of the horns. To adjust the angle of the horn, one must unscrew the shell from the frame, tilt the horn to the desired position, and then screw down the shell to the structure. The torque exerted by the screwing motion is significant enough to potentially move the shell from its set position. This results in a tedious calibration process and detracts from the effectiveness of the design.

Lastly, the current horn holding design is presenting a compressive force against the horn in order to keep it in place. This is problematic because, in some cases, the horns are warping and deforming due to this force. As shown in figure-19 one can see that the bottom lip of the horn is deformed. This is not ideal for transmitting or receiving a radio frequency because the warped

shell can potentially distort the trajectory, thus skewing data or making it difficult to hit the desired target. It is also possible for the horns to crack. Since they are made of an inexpensive plastic material, the horns lack the strength to withstand strong compressive forces.

To amend these issues with the current design, Mechanical Engineering team #18 has been working on multiple concepts, alongside the two mechanical engineers on our team. Three preliminary designs were generated, all of which address the concern of being able to adjust the horns with two degrees of rotational freedom. After deliberation with Northrop Grumman, one concept was selected as a preferred design and will now be discussed in further detail.

Displayed below in figure-19 is the improved horn holder design. This concept allows for the two degrees of rotational freedom needed, something not achieved in the current design. Its fulcrum point is located near the center of the horn so that adjustments to the angle will be as accurate as possible while calibrating the horn. This is equivalent to a fulcrum point located at the rear of the horn, making micro adjustments difficult because a minimal rotation at the rear of the horn would translate into a large rotation at the front of the horn. This design also allows for a laser to be attached, making for a more efficient calibration process. Further, the design is to be compatible with the 80/20 fasteners allowing for easy mounting of each horn. This is because, the structural redesign will utilize the 80/20 extruded aluminum.

However, there are still some factors that need to be considered before manufacturing begins. Firstly the actual locking mechanism design has not been finalized. This is a critical aspect of the design as to avoid the inaccuracy and tediousness from 2014's prototype. The locking mechanism must be smooth and minimize the possibility of moving the horn from its desired position. Secondly, the design is quite complex and will most likely have to be custom made. This translates into a higher cost than a commercial off-the-shelf item, as well as makes the design process more involved in order to ensure accuracy.

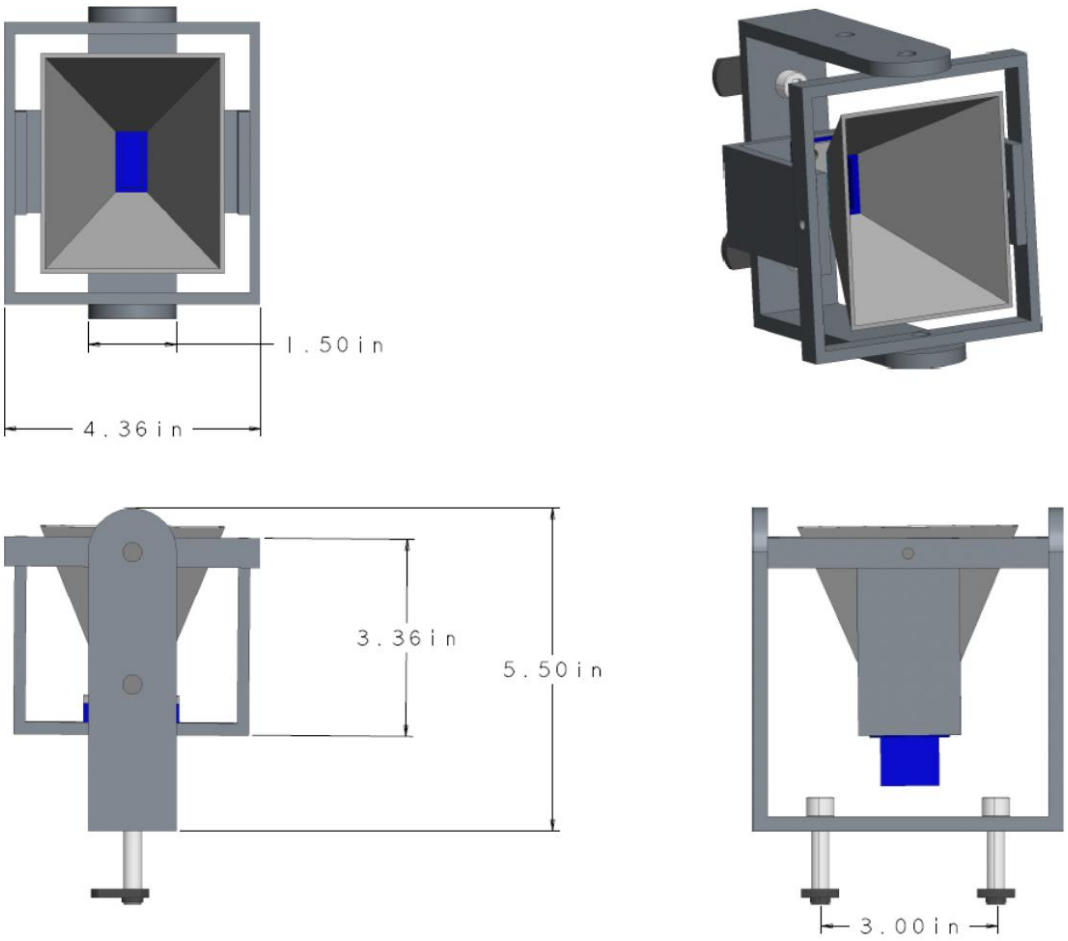

Figure 19- Cad image of the improved horn holder design

3.2.10 Component Box

The component box houses all of the electrical components with the exception of a laptop and a monitor screen. The box will mount on the back of the radar structure, making it a self-contained system. The weight of the box should be minimal while maintaining easy access to all components for testing purposes.

Figure 20 – Image of the current component box

The current box seen in figure 20 is of an “L” shape open to the air allowing for sufficient cooling. Made of both steel and aluminum, this design is too heavy and cumbersome. It attaches to the frame with a slot and pin-type system where rectangular pins extrude from the frame. The matching rectangular slots on the box allow for the two to connect. This design relies on friction and gravity with no real locking mechanism, making it potentially dangerous to the radar itself and the users around it.

The new box seen in figure 21 will be constructed from lightweight ¼” acrylic panels. It will bolt onto the back of the frame allowing for a safe and secure connection. Additionally the components will be raised off the panel to allow for easy cable assembly as well as proper cool of each of the components. This design incorporates a lid to add a layer of protection to the components as well as double as a surface to set the laptop and monitor on during operation.

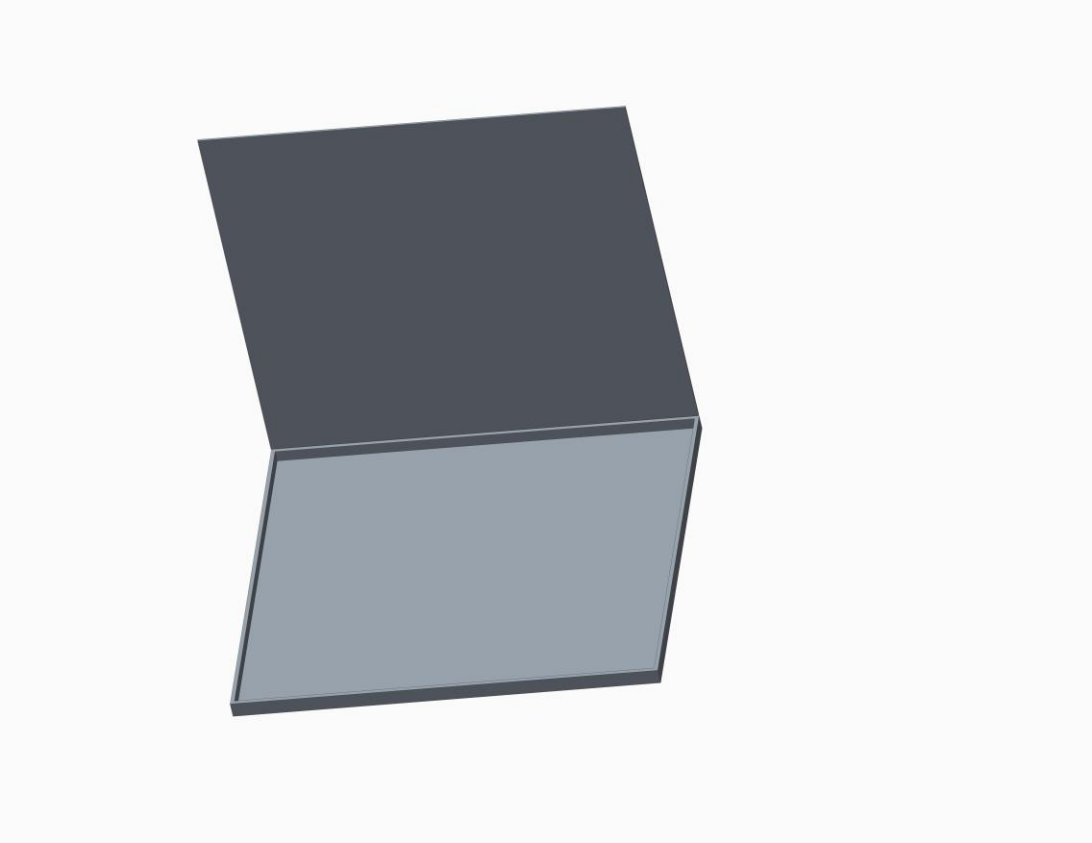

Figure 21 – CAD image of gen 2 component box

3.3 Thermal Analysis

3.3.1 Thermal Analysis of Component Box

To begin thermal analysis on the component box, the first step was to determine the amount of power supplied to each component to understand how much heat must be dissipated. By adding each electrical component’s power supply, we received a value of 34.8W. Next, obtaining the inside surface area of the box will allow us to obtain the heat flux by dividing

the input power over the total inside surface area. As of now, the calculated inside surface area is 12.54ft2. This introduces a heat flux value of approximately 2.77W/ft2. Lastly, using Fig. 22 as shown below, one can obtain the rise in temperature inside the enclosure by assuming an “unfinished aluminum and steel enclosure” giving us a value of approximately 15 C. This concludes that the temperature inside the enclosure is about 15Chigher than ambient temperature, which is taken as 75C. This equates to an enclosure temperature of 90C.

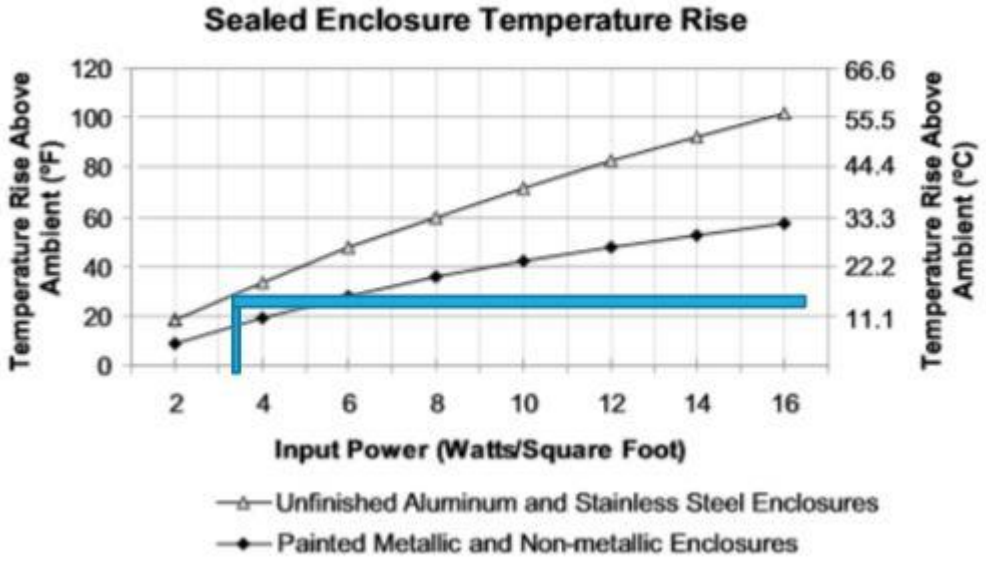

Figure 22 – Temperature Rise within Enclosures

Once these two temperatures are determined, one is able to begin the thermal analysis to ensure that the 34.8 W produced by the electrical components can be safely dissipated through the component box given the geometry and material selection. The approach used was a thermal resistance network to analyze each surface of the box individually. To conduct this analysis, one-dimensional steady-state heat transfer was assumed in order to simplify the calculations. This analysis is analogous to an electrical circuit where the heat is related to the current, the temperature difference as the voltage and the electrical resistance to the thermal resistance. Each side consists of three separate thermal resistances: convection from the electrical components surface to the inner surface of the box, conduction through the actual material, and lastly, convection from the outside surface of the box to its surroundings. In this case, the thermal resistances are all in series and thus are summed to obtain a total thermal resistance. The total thermal resistance is defined in Eq. 5 which includes all three

intermediate thermal resistances. The "h" in the equation is the natural heat convection coefficient and the "A" is the surface area of the box in which the heat is dissipating through. Using the thermal resistance network approach, the heat transfer is equal to the temperature difference over the sum of the thermal resistances in series, as shown in Eq. 6.

$$R_{total}=\frac{1}{h_{1A}}+\frac{1}{k_A}+\frac{1}{h_{2A}} \tag{5}$$

$$Q_{total}=\frac{T_{\infty 1}-T_{\infty 2}}{R_{total}} \tag{6}$$

The heat dissipated through each of the six sides was calculated and summed to be approximately 155 W. This clearly exceeds the required heat dissipation of 34.8 W and provides a factor of safety of about 4.5. This deems the component box geometry and material to be safe and appropriate to house the electrical components.

4 Methodology

4.1 Schedule

Given the magnitude and complexity of the project, a considerable amount of time in Semester I (Fall 2015) is allocated to team self-education and understanding of the SAR's fundamentals of operation. Verifying and troubleshooting the current product is critical to establishing a sound foundation for further design and development, so thorough testing protocols are a major part of the schedule, not just for Semester I, but also moving into the beginning of Semester II (Spring 2016). Fabrication and implementation of new designs will be executed primarily in Semester II.

4.1.1 Gantt Chart

	Task Name	Duration	Start	Finish
1	**Planning**	**53 days**	**Tue 9/22/15**	**Wed 12/2/15**
2	NG Technical Briefing: Top-Down, Electrical System	1 day	Tue 9/22/15	Tue 9/22/15
3	NG Technical Briefing: Antenna Design Considerations	1 day	Mon 9/28/15	Mon 9/28/15
4	NG Technical Briefing: Image Formation & Processing	1 day	Tue 10/6/15	Tue 10/6/15
5	NG Technical Briefing: ADC, IQ Demod	1 day	Tue 10/13/15	Tue 10/13/15
6	Electronics Testing Strategic Plan	1 day	Fri 10/16/15	Fri 10/16/15
7	NG Technical Briefing: Degrading Lobes, Ambiguous Image	1 day	Tue 10/20/15	Tue 10/20/15
8	Northrop Grumman In-person Consulting	1 day	Sat 10/31/15	Sat 10/31/15
9	Semester II Strategic Plan	1 day	Tue 12/1/15	Tue 12/1/15
10	**Electronics Testing, Troubleshooting & Evaluation**	**40 days**	**Fri 10/9/15**	**Wed 12/2/15**
11	Equipment Inventory	1 day	Fri 10/16/15	Fri 10/16/15
12	Test Plan FA15-FAM-000	1 day	Sat 10/31/15	Sat 10/31/15
13	Test Plans 000 - 008	2 wks	Mon 11/2/15	Fri 11/13/15
14	Test FA15-TXIF-009: VCO	2 wks	Mon 11/16/15	Fri 11/27/15
15	Evaluate Test Results and Develop Reccomendations	1 day	Mon 11/30/15	Mon 11/30/15
16	**Software Development**	**40 days**	**Fri 10/9/15**	**Wed 12/2/15**
17	Top-Level I/O Definitions & Functional Diagrams	2 days	Mon 11/2/15	Tue 11/3/15
18	Subroutines & Functions I/O & Functional Diagrams	1 wk	Wed 11/4/15	Tue 11/10/15
19	Pseudocode & State Diagrams	3 wks	Wed 11/11/15	Tue 12/1/15
20	Assign Coding Tasks & Responsibilities	1 day	Wed 12/2/15	Wed 12/2/15

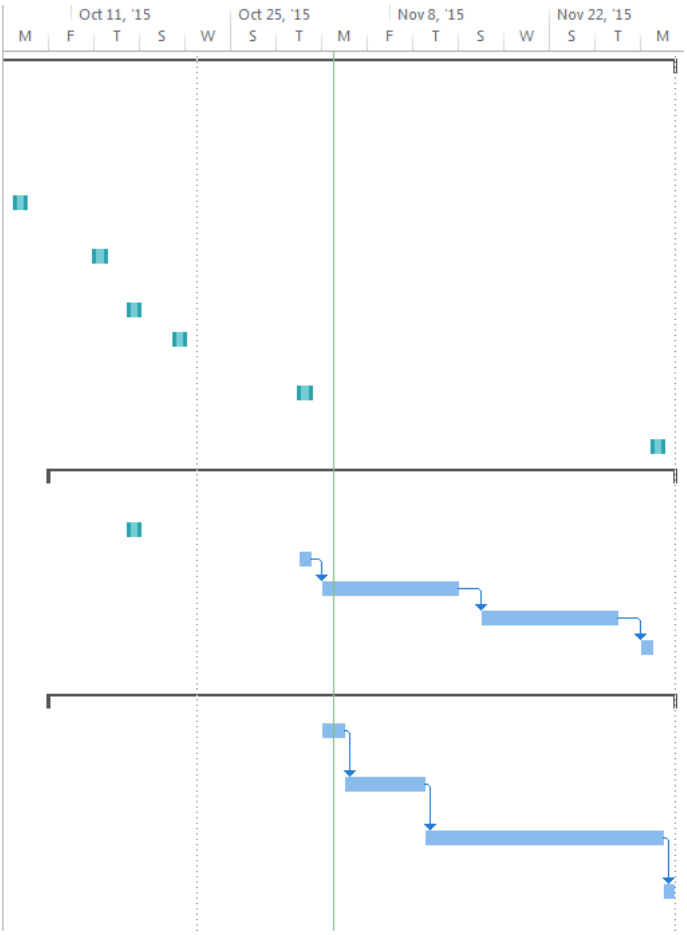

Figure 10 – Fall 2015 Semester Gantt Chart

4.2 Resource allocation

Having a multidisciplinary team is beneficial in terms of resource allocation because there are more resources available by combining departments. This combination allows the team to have access to two different labs to work in. Having this access will increase the team's efficiency by allowing the team to split tasks and work on separate tasks at the same time as well as decreasing the risk of having to wait for room availability. Our team has a budget an initial $5,000 provided by Northrop Grumman. If need be, the budget can be stretched to $10,000 but it is in the team's best interest to minimize cost and not to exceed the original budget. This budget will be spent strategically between the electrical components and the manufacturing of a component box.

Fortunately, the team is able to reuse last year's prototype which contains many of the electrical components required. Because these electrical components are rather expensive, the team will ensure that the existing components are functioning and, if not, can be repaired by the manufacturer. For the manufacturing of the component box, comparisons will be made between vendors and distributors to ensure that costs are appropriate and as economical as possible. The team is also able to take advantage of the machine shop available at the College of Engineering. This will eliminate any money needed for fabrication, allowing the money to be focused on the material itself. Alternatively, if the component box can be configured to the redesigned structure such that it does not have to be custom made then the cost and time would decrease drastically.

4.2.1 Human Resources & Roles

Scott Nicewonger

Project Manager & RF Engineer

It is the role of the Project Manager to ensure that all deadlines are met in a timely fashion and that all milestone objectives are achieved. The Project Manager is involved with the risk/issue analysis of all design phases; coordinates with each working group of the team; coordinates with faculty, sponsors, and third parties/vendors; ensures resource allocation and availability; and delegates' tasks to team members and working groups judiciously and fairly.

The RF Engineer, first and foremost, ensures that any radio frequency energy emitted by any product, prototype, or device is not harmful to humans as defined by ANSI/IEEE C95.1-1992 guidelines and FCC Rules and Regulations 47 C.F.R. 1.1307(b), 1.1310, 2.1091, 2.1093. Furthermore, the RF Engineer ensures the product operates within the customer's RF transmit and

receive specifications, as well as carefully considering design issues of RF propagation and RF interference.

Critical Skillsets: RF Comms Troubleshooting, Field Theory

Kegan Stack

Lead Mechanical Engineer

The Lead Mechanical Engineer provides the Project Manager with the particular specifications and limitations of the Imager as they pertain to design and structure of the Imager and its components. The Lead Mechanical Engineer is the primary liaison to ME Team #18, and along with the Project Manager, ensures ME Team #18 products and designs are compatible with ECE Department requirements.

The Lead Mechanical Engineer supervises the optimization of the design of the antenna configuration and the structure to hold the antenna as well as the electrical components for weight, size and portability. Using both CAD and Professional Engineering Software, mechanical engineers produce precise models and drawings. Sole responsibility for the material used to produce the structure will fall among the mechanical engineers. They work in close proximity to the RF Engineer to make sure the system is physically working properly.

Critical Skillsets: AutoCAD, FEA and Thermal Fluid Analysis

Olivier Barbier

Lead Programmer

The Lead Programmer is responsible for software code deliverables and works closely with the Signal Processing Engineer during implementation. The Lead Programmer delegates programming tasks to team members as appropriate and is responsible for Quality Assurance of all programming products.

Critical Skillsets: Programming & Filters

Jordan Bolduc

Secretary, Webmaster & Signal Processing Engineer

It is the role of the Secretary to keep track of the minutes and document the weekly meetings. The webmaster is responsible for ensuring that all needed information and files are available on the team's website.

The Signal Processing Engineer is responsible for the accuracy and efficacy of the mathematical calculations and models which will be used to resolve received signals into useful data. The Signal Processing Engineer works closely with the Lead Programmer to ensure signal processing models are implemented into software successfully.

Critical Skillsets: Signal Analysis, Field Theory and Soldering

Julian Rodriguez

Treasurer, Procurement Manager & Mechanical Engineer

It is the role of the Treasurer to manage all monies and budgetary concerns for the project to guarantee that the tasks are performed at the lowest cost possible to achieve the highest necessary performance as stated in the objectives of the product requirements.

The Procurement Manager is responsible for ensuring that components are purchased in the most efficient and economical manner. The Procurement Manager works closely with both the department and sponsor to ensure time is not wasted waiting on material.

The Mechanical Engineer ensures structural integrity and an efficient design of the antenna and associated mechanical products. As a member of an Electrical Engineering Department led team, the Mechanical Engineer collaborates with electrical and computer engineers as well as with ME Team #18.

Critical Skillsets: CAD, FEA, Design, & Thermal Fluid Analysis

4.3 Risks & Uncertainty

With any planned design, there comes a risk of unseen factors that can potentially cause problems or a delay, requiring a greater effort to work around later on. Being able to predict and keep in mind potential risks and uncertainties will aid in the design process by preventative planning. Currently, the team is still in the design phase as well as the testing phase. In the design phase, there runs the risk of having a model in CAD which seems ideal however might not work

out once the prototype has been constructed. Some risks as of now include the horn holders. Although the design appears sound, it is possible that there might be interference with the cables once the horns are attached and configured.

Other upcoming tasks that hold uncertainty include deciphering and debugging the code produced by last year's team. Since there are many ways to write code and think through the logic, it might prove challenging to follow someone else's thought process. Also, there is always risk whenever working with electrical components. An obvious risk from working with electricity is being electrocuted.

Some other uncertainties include the testing of the electrical components. Currently, the testing phase has not yet been completed so there are still many components whose status remain unknown. It is the team's duty to test each component to determine what needs to be replaced or repaired ahead of time because if a critical part is not working, then there will be a window of wasted time until it is replaced. Much of the electrical hardware is expensive, so it is the team's responsibility to allocate the budget correctly to ensure that the components are in working order without exceeding the funding provided. Lastly, there lies uncertainties in keeping the weight of the structure down while still maintaining stability. As of now, finite element analysis has not yet been completed. Completing this analysis will determine if the aluminum will be strong enough to support the weight of itself as well as the weight of all the components.

5 Conclusion

This project came with a steep learning curve. Although a considerable amount of time was spent on learning the concepts of operation and evaluating the generation 1 design, the team has made key value-added contributions to the project which will set the stage for Semester II.
Top-level I/O definitions and the functional diagram for the FPGA was developed, providing a road map for crucial VHDL coding tasks that were not realized in the generation 1 design. Subsystems for analog to digital conversion (ADC), complex multiplication, image display, and system timing have been defined and are ready for coding to begin in earnest. In particular, the ADC modules have already passed the first battery of testing (FA15-CTRL-001).

While the 2014 team implemented signal processing calculations in Microsoft Excel spreadsheet format, the algorithm decided upon in Sec 3.2 Fig 4 will enable the realization of signal processing in the FPGA, rather than in an external system.

While the FPGA development has progressed ahead of schedule, troubleshooting the low power output and frequency of the voltage-controlled oscillator (VCO) has not progressed as hoped. The VCO purchased by the 2014 team operates on a proprietary software suite which the team will have to dedicate time resources to learning. Given the critical nature of this component to the design's independent functionality, solving this problem will be a top priority in the interim, and moving into Semester II.

Over Winter break, the Lead Programmer and Signal Processing Engineer will continue to develop the code modules assigned to them remotely. The RF Engineer will focus on VCO functionality, switch verification, and signal flow verification. Additionally, open-source course material on radar systems engineering has been assigned as mandatory professional development. Semester II will begin with evaluation and critical path analysis. The specific tasks and dependencies will depend on the state of FPGA functionality achieved over the Winter break, but considerable bench testing according to Test Plan 6.3 will be necessary. ME Team 18 will begin fabrication and construction of the structure in parallel to the ECE work. Test Plan FA15-TXRX-015: Tx-Rx Delay Line Hard Loopback will ensure that any electrical system testing or development, short of actual down-range RF transmission testing, can be accomplished on the bench, without disrupting the workflow of either team.

The end goal of the project remains to be the successful design and implementation of a synthetic aperture radar imaging system which safely and accurately detects a metal target from a distance of 20 feet, independent of external signal or timing sources, and maps the downrange energy scattering to a VGA display. To that end, the SAR Imager Team is progressing on schedule.

6 Appendix A – Reserved for Electrical needs

6.1 Requirements

6.1.1 Functional Requirements

- REQF-001: Frequency Range
    - The frequency range of the imager should be within FAMU-FSU College of Engineering policies. The SAR will emit 10 GHz X-band energy at low power levels.
- REQF-002: Operating Range
    - The range from the imager to the target needs to be 20 feet.
- REQF-003: Extent of the Scene
    - The area that must be imaged should be the width of a normal sized person.
- REQF-004: Cross Range Resolution
    - The cross range resolution must be enough to discern whether there is a possible threat by showing there is large scatter on a specific portion of the body, but it need not be sharp enough to outline the particular type of weapon. The designed pixels size to divide the scene into would be 2.5 inches x 2.5 inches.
- REQF-005: Down Range Resolution
    - Down range resolution will be a future capability. For ethical reasons, the down range resolution should not be so high as to be capable of producing a high-resolution image of the human body.
- REQF-006: Pulse Width
    - The pulse width is nominally 20 ns since target (20 feet away) round trip is 40nS away as pulse travels 1nS per foot leaving 20nS for system to switch to receive mode at the end of the transmit pulse to detect the reflected pulse .
- REQF-007: Voltage Controlled Oscillator
    - The VCO used for converting the signal must be functional at 5 GHz.

6.1.2 Non-Functional Requirements

- REQN-001: FCC Rule and Regulation
    - The Radio Frequency (RF) emitted from the SAR imager must be within ANSI/IEEE C95.1-1992 guidelines and FCC Rules and Regulations 47 C.F.R. 1.1307(b), 1.1310, 2.1091, 2.1093 regarding safe RF exposure for humans.
- REQN-002: Components Interference
    - The Radio Frequency (RF) from the SAR imager should not affect communication between any other electrical components in the design.
- REQN-003: Interference
    - The Radio Frequency (RF) from the SAR imager should not interfere with common communications systems in the environment.
- REQN-004: Logic Implementation
    - The programing language used to communicate with the FPGA should be VHDL.

6.1.3 Mechanical Functional Requirements

- REQM-001: Structural Redesign
    - The redesigned structure should be optimized for weight and stability. This includes a target weight goal of 80 lbs. Must still maintain rigidity. Increase the structure's mobility, preferably by introducing wheels to the structure.
- REQM-002: Horn Calibration
    - Horns must be adjustable in both azimuth and elevation angles. Horn's angular setting must be within 5 degrees. Tolerance must be less than 1/10th of an inch. Must focus within a circle of 1ft diameter from 20 ft. away.
- REQM-003: Component Box
    - Component box must dissipate the heat generated by the electrical hardware. Its weight and size must also decrease while being configured to the newly designed structure.

6.2 Implementation Considerations

- ICON-001:
  - The SAR imager should primarily use commercial-off-the-shelf (COTS) components to facilitate production cost effectiveness.
- ICON-002:
  - The final prototype should be evaluated using National Institute for Occupational Safety and Health Work Practices Guidelines (NISOH) and/or U.S. Military Standard 1472 F to determine a recommendation for safe manual lifting.
- ICON-003:
  - All purchases should not exceed the allocated budget amount of $10,000.

6.3 Test Plans

Test Identifier	Title	Description
FA15-FAM-000	Test Equipment Familiarization & Safety	Feed Pulse Generator directly to Spectrum Analyzer. Study Span, ResBW, PRF spectral lines, envelope, etc.
FA15-CTRL-001	FPGA ADC Input Voltage	Apply voltage from 0 – 3.3 V to FPGA PMOD pins & verify 12-bit hex words on 7-seg display.
FA15-CTRL-002	FPGA Switching Logic	Use slider switches on FPGA board to simulate every switching state.
FA15-TXRF-003, A-F	TX Output Power & Gain (Constant)	Verify RF power of each component along TX Path to PA w/constant source. No Switching, No Timing.
FA15-TXLO-004, A-D	LO Output Power & Gain (Constant)	Verify IF power of each component along LO Path up to IQ Demod w/constant source. No Switching, No Timing.
FA15-RXRF-005, A-D	RX Power & Gain (Constant)	Verify RF power and gain from BPF to IQ Demod w/constant source. No Switching, No Timing.

FA15-TXIF-006	SPDT Switching (Manual)	Use FPGA slider switch controls to verify both switch paths.
FA15-TXRF-007	SP4T Switching (Manual)	Use FPGA slider switch controls to verify all switch paths.
FA15-RXRF-008	SP16T Switching (Manual)	Use FPGA slider switch controls to verify all switch paths.
FA15-TXIF-009	VCO	Generate 5GHz, -4dBm signal from VCO.
FA15-CTRL-010	FPGA Fast Pulse	Verify FPGA 50MHz, 0.333 duty operational pulse.
FA15-TXIF-011	IF Output Power And Pulse Fidelity of SPDT Switch w/ VCO & FPGA fast pulse	Verify output power and pulse fidelity to TX/LO common SPDT using VCO and FPGA fast pulse.
FA15-LORF-012, A-D	LO Power & Pulse Fidelity w/ VCO & FPGA fast pulse	Verify RF power & pulse fidelity along LO Path using VCO and FPGA fast pulse.
FA15-TXRF-013, A-J	TX Output Power & Pulse Fidelity	Verify RF power & pulse fidelity along TX Path using VCO and FPGA fast pulse
FA15-RXRF-014	RX Gain & Pulse Fidelity	Verify RF power and gain to IQ Demod (including SP16T) using VCO and FPGA fast pulse.
FA15-TXRX-015	Tx-Rx Delay Line Hard Loopback	Match coax length such that line propagation delay matches RF to target and return propagation delay. Tx/Rx hard loops. May need a variable attenuator.

6.4 Cellular RAM Chips Waveform Diagram

The table shows a description of the signal required to implement a RAM storage on the FPGA.

VFBGA Assignment	Symbol	Type	Description
G2, H1, D3, E4, F4, F3, G4, G3, H5, H4, H3, H2, D4, C4, C3, B4, B3, A5, A4, A3	A[19:0]	Input	Address Inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the bus configuration register or the refresh configuration register.
J2	CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static LOW or HIGH during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations.
J3	ADV#	Input	Address valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# can be held LOW during asynchronous READ and WRITE operations.
A6	CRE	Input	Configuration register enable: When CRE is HIGH, WRITE operations load the refresh configuration register or bus configuration register.
B5	CE#	Input	Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode.
A2	OE#	Input	Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	Write enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
A1	LB#	Input	Lower byte enable: DQ[7:0].
B2	UB#	Input	Upper byte enable: DQ[15:8].
G1, F1, F2, E2, D2, C2, C1, B1, G6, F6, F5, E5, D5, C6, C5, B6	DQ[15:0]	Input/ Output	Data Inputs/outputs.
J1	WAIT	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between REFRESH and READ/WRITE operations. WAIT is asserted when a burst crosses a row boundary. WAIT is also used to mask the delay associated with opening a new internal page. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH.
E3, H6, J4, J5, J6	NC	–	Not internally connected.
D6	V_{CC}	Supply	Device power supply (1.7–1.95V): Power supply for device core operation.
E1	V_{CCQ}	Supply	I/O power supply (1.7–3.6V): Power supply for input/output buffers.
E6	V_{SS}	Supply	V_{SS} must be connected to ground.
D1	V_{SSQ}	Supply	V_{SSQ} must be connected to ground.

Note: The CLK and ADV# inputs can be tied to V_{SS} if the device is always operating in asynchronous or page mode. WAIT will be asserted but should be ignored during asynchronous and page mode operations.

The following figure show those controlled signal flow